IN THE CLAIMS

Please cancel Claims 7-10 without prejudiced and amend Claims 1 and 11 as shown in marked-up form as follows:

1. (Currently Amended) A tunable quadrature phase shifter, comprising:

an input means for inputting an input signal;

splitting means for splitting the input signal into two essentially orthogonal first and second signals;

adding means for adding said first and second signals;

subtracting means for subtracting said first and second signals;

a first output for outputting a first output signal based on the output signal from said adding means; and

a second output for outputting a second output signal based on the output signal from said subtracting means,

wherein said splitting means is an all-pass having a time constant of C/g_m, where C is a capacitance in the subtracting means and g_m is the transconductance of the subtracting means.

2. (Previously Presented) The phase shifter of claim 1, further comprising a first output buffer means for buffering said first

output signal, and a second output buffer means for buffering said second output signal.

3. (Previously Presented) The phase shifter of claim 1, further comprising a first transimpedance converter having its input connected to said input means.

4. (Previously Presented) The phase shifter of claim 1, further comprising a first transimpedance converter having its output connected to said first output, and a second transimpedance converter having its output connected to said second output.

5. (Previously Presented) The phase shifter of claim 3, wherein the transimpedance converter is a transimpedance amplifier.

6. (Previously Presented) The phase shifter of claim 2, wherein said first and second output buffer means are first and second transimpedance converters, respectively.

7-10 (Cancelled)

11. (Currently Amended) A data and clock recovery unit comprising a phase detector which includes a phase shifter having

an input means for inputting an input signal;

splitting means for splitting the input signal into two essentially orthogonal first and second signals;

adding means for adding said first and second signals;

subtracting means for subtracting said first and second signals;

a first output for outputting a first output signal based on the output signal from said adding means; and

a second output for outputting a second output signal based on the output signal from said subtracting means,

wherein said splitting means is an all-pass having a time constant of C/g_m, where C is a capacitance in the subtracting means and g_m is the transconductance of the subtracting means.